

**A Design Approach to Optimize Hybrid Voltage Regulators**: Dense, power-efficient 48V-to-1V voltage regulators, embedded near points-of-load rather than mounted on a printed circuit board, are needed to support the high-power, high-current density needs of next-generation high-performance computing systems. These integrated power delivery solutions, or hybrid voltage regulators (HVRs), must support the dual requirements of increased functionality in a small form factor, and reduced energy and power consumption. However, the ad hoc simulation-based design approaches used thus far with HVRs fundamentally limit the optimization of HVR circuit architectures and sizing. To address this, University of Illinois researchers will present a generalized HVR architecture, analytical model, and design optimization methodology at ECTC. They compared their analytical power loss calculations to simulation results from commercially available simulation software, and saw more than 92.87% accuracy across all the HVR architectures studied. They studied tradeoffs of power efficiency vs. density based on various proposed models, as well as approaches to enhance the power efficiency of existing HVRs. As a result, they will propose at ECTC a design methodology that considers a) the number of components and sharing of inductors among switching branches, and b) the balancing of various types of HVR power losses through the use of optimal design parameters in a multi-step optimization process that has shown over 8% reduction in total power loss.

* **The graphs above** show the results of the multi-step design optimization process for both dual-phase multi-inductor hybrid (DPMIH) and dual switched capacitor hybrid (DSCH) HVR architectures. (a) shows that redesign of high-side (HS) switches yields a $∼$6% reduction in power loss, while (b) shows that optimization of the switching frequency yields an additional $∼$2-2.5% reduction in power loss.

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